Power Electronics

Laboratory Exercise # 1

Flyback Converter

The Flyback-converter - description of the building blocks

The Flyback-converter investigated in the laboratory, is a commercially available switch mode power supply. This means that several of the circuit solutions becomes somewhat complicated, especially regarding the control. The reason is that commercial products should work satisfying without being expensive to manufacture. Since the voltage controller is very complicated, the investigation is instead focused on the power electronic main circuit. Note the 0.1 Ω resistors placed in the main circuit shown in the drawing. These are intended for current measurement. Since test points are placed on both sides of the resistors, the current measurements are carried out as differential voltage measurements.

It is of great importance where the probe ground connection is placed. This is due to the fact that the measurement reference voltages on either sides of the switch transformer are at galvanically separated potential levels. Therefore, only one of the ground connections of the probes must be used. If two are used, the corresponding two potentials are short circuited inside the oscilloscope. As a consequence it is advisory to first make all the measurements on one side of the galvanic cut and then on the other. If signals on both sides of the switch-transformer should be studied at the same time, differential measurements should be adopted.

The Flyback-converter main circuit

The Flyback-converter main circuit, including snubber circuits, is shown in Figure 1. At the converter input, a filter is placed, consequently termed input filter. The capacitor and resistor together forms a differential mode (DM) filter. This filter attenuates electronic noise affecting the phase and the neutral lead, if the disturbances do not have the same sign and magnitude for both leads.

The transformer connected after, forms a common mode (CM) filter, which attenuates disturbances if they do not affect the phase and neutral with equal magnitude and opposite sign. After the transformer another DM-filter is placed, consisting of two capacitors. The middle point earth connection shown, is not used in the laboratory set-up. After the first DM-filter a component marked T-, is inserted. This is a negative temperature coefficient (NTC) resistor, whose resistance decreases with increasing temperature. This is needed in order to limit the inrush current otherwise appearing when the converter is connected to the power grid. The input filter is followed by the diode rectifier and the DC link capacitors.

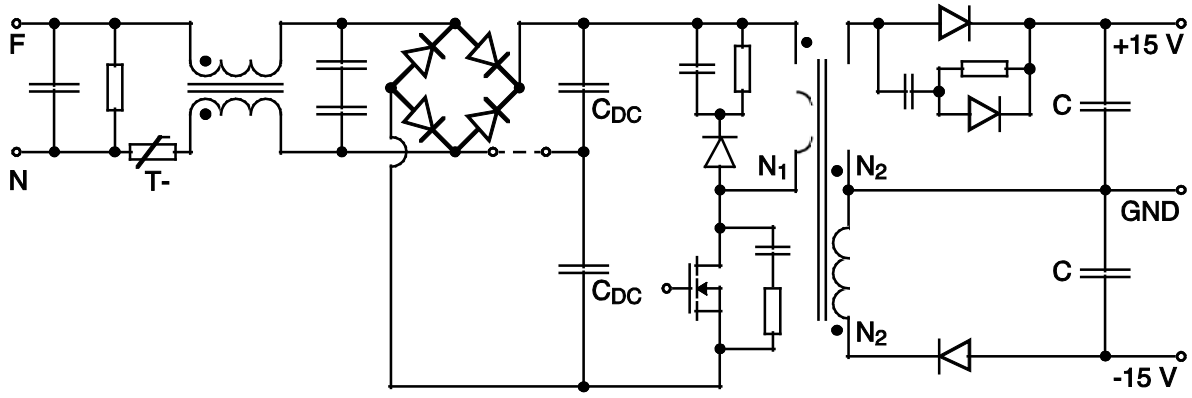


Figure 1 The power electronic main circuit of the Flyback-converter including snubber circuits.

Since the power supply should also be used in countries with 115 V phase to neutral voltage, the DC link capacitor connection to the diode rectifier is variable, which is marked as a dashed line in Figure 1. At 115 V operation, the points connected by this line is connected also electrically. The result is that during positive half period of the grid voltage, one of the DC link capacitors is charged, whereas during the negative the other one is being charged. This means that the DC link

voltage magnitude are equal for both 115 V and 230 V phase to neutral voltage. Note that if the connection discussed above is made, only two of the rectifier bridge diodes are used.

The switch-transformer is connected in series with the switch-transistor, in this case a MOSFET, across the DC link. The switch-transformer has in this case two secondary windings, since the output voltage should be ±15 V DC. In some cases the secondary is equipped with three windings to also have a +5 V DC output. The difference compared to the case with only one secondary winding is that the total energy supplied to the secondary is split among several windings, instead of only one. The secondary windings have one common point to which they are connected, to create the output reference potential (ground).

In series with the other two secondary leads, the switch-diodes are connected. Between the diodes and the output, the output filters are inserted. These are of CLC-type, which compared to a purely capacitive C-filter, has a better attenuation of high frequency voltage ripple caused by switching. No attention is paid to the CLC-filter, it can be regarded as being purely capacitive, i.e. consisting of only a capacitor.

Note that the +15 V output voltage is controlled while the –15 V output is not. This is common to all Flyback-converters having several secondary windings. This is due to the fact that the only control parameter available is the switch transistor duty-cycle, which implies that only one quantity can be controlled. In this case, the +15 V output voltage is controlled, which is termed MASTER. The uncontrolled –15 V output is referred to as the SLAVE.

Snubber circuits

In Figure 1, three snubber circuits are plotted. Only one of them is of standard type, the RC-snubber connected across the switch transistor. The other two is more unusual. One of them, connected across the switch-transformer primary, is intended to provide an alternative path for the transformer primary current at the MOSFET turn-off transient. This is needed due to the fact that energy is stored in the transformer primary leakage inductance. This energy cannot be transferred to the secondary since the leakage inductance on the primary has no magnetic connection to the secondary. Therefore, a discharge path should be provided, which the snubber does. At MOSFET turn-off, the energy stored in the primary leakage inductance is transferred to the snubber capacitor. Then the snubber capacitor is discharged through the snubber resistor.

Note that the time constant of this RC-circuit is fairly long. As a matter of fact it is selected so long that the capacitor voltage do not decrease to a level lower than the primary side transformer voltage when the switch-transistor is in the off state. Since the latter voltage is negative the snubber capacitor otherwise would be charged from the primary.

The other unknown snubber circuit is connected across the MASTER Flyback-diode. This snubber is essentially capacitive but also equipped with a snubber diode and resistor. It reminds of a common RCD-snubber with the difference that the snubber diode is connected in the opposite direction.

Control

The supply voltage for the control electronics is created by dividing the DC link voltage. This is performed by a resistive voltage divider connected in series with a 12 V zener-diode. To transfer a fault signal from the output side to the control side the opto-coupler 151 is used. If the MASTER DC voltage exceeds 18 V, the opto-coupler 151 is trigged.

The thyristor 43 is trigged by the opto-coupler 151, which causes short circuit of the 12 V control electronics supply. This in turn inhibits the transistor switching. The thyristor 43 cannot be turned off, unless the converter is disconnected from the grid, since its anode current cannot commutate in other ways. If the SLAVE DC voltage becomes lower than –18 V, the zener diode 46 starts conducting, but this is not transferred or by other means dealt with.

To transfer the measured MASTER output voltage to the control side, the opto-coupler 150 is used. The anode on the input side of the opto-coupler 150, is connected to the MASTER positive potential. The cathode on the input side of the opto-coupler 150 is connected to a reference diode

and via a resistor down to the output side common (ground). The voltage across the reference diode is adjustable by varying the resistance of the potentiometer 170. This reference diode can thus be treated as an adjustable zener diode. The output side of the opto-coupler 150 is connected to an oscillator circuit, which generates control pulses to the switch-transistor.

The oscillator and the transistor drive circuit are shown in Figure 2. To understand the operation of the oscillator circuit, it must be realised that the inverters 40, are CMOS integrated circuits, and therefore have an input capacitance corresponding to some tens of pF. Furthermore, there are diodes connected between the input and the both supply voltages which means that the input voltage cannot exceed 12 V or be lower than the reference potential (0 V). Also it must be clear that the switch state is changed at the discrete voltage levels V_{IL} and V_{IH}.

In order to simplify the analysis, the oscillator is redrawn to include the input capacitance and the input diodes for the leftmost inverter. Therefore, the inverters can be regarded as ideal from now on. The simplified oscillator is shown in Figure 3.

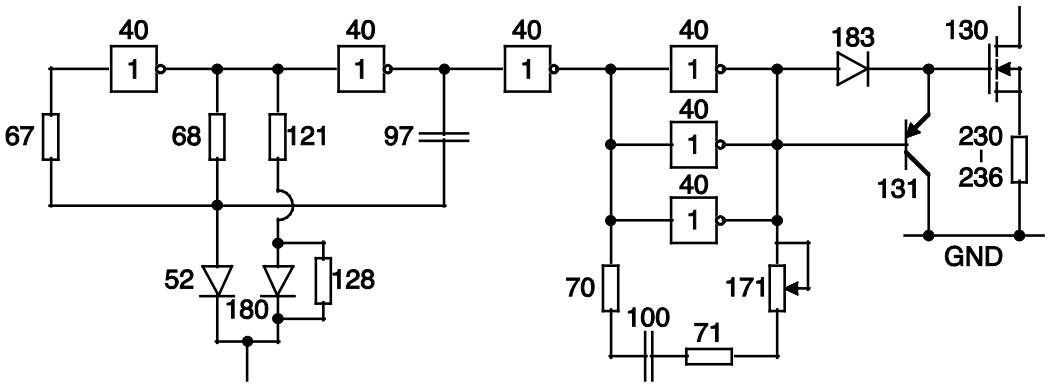


Figure 2 The oscillator and drive circuit of the Flyback-converter.

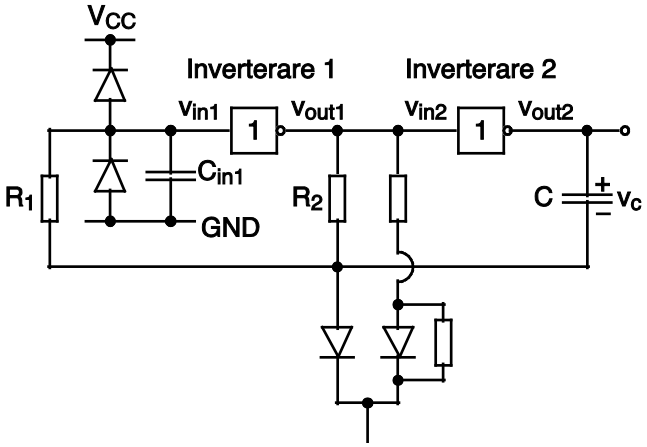


Figure 3 The simplified oscillator.

Assume that the analysis starts at v_{in1}=0 V, i.e. C_{in1} completely discharged. Consequently, v_{out1}=v_{in2}=12 V and v_{out2}=0 V. This means that C_{in1} is being charged through R_1+R_2 and C is charged (to a negative voltage) via R_2. When v_{in1} reaches the threshold level V_{IH}, a change of the output state is generated in such a way that v_{out1}=v_{in2}=0 V which gives v_{out2}=12 V. Since the capacitor C is charged to a negative voltage, the voltage v_{in1} will increase to 12 V abruptly, when the inverter 2 changes output level, due to the voltage across capacitor C. The remaining charge stored in C, is being discharged to the 12 V supply voltage via the upper input diode of inverter 1.

Now, C_{in1} is instead discharged against v_{out1} via R_1+R_2. Also, C is being charged to a positive voltage via R_2. When v_{in1} reaches the threshold level V_{IL}, a change of state is generated at its output such that $v_{out1}=v_{in2}=12$ V which gives $v_{out2}=0$ V. In this case the capacitor C is charged to a positive voltage. Consequently, the inverter 2 output voltage affects the inverter1 input voltage in such a way that it becomes 0 V. The remaining charge of capacitor C is discharged to signal ground through the lower input diode of inverter 1.

This concludes the analysis of the oscillator circuit, since the last state entered is equal to the initial state from which the analysis started. The opto-coupler 150 can affect the duration of the charging intervals discussed above. If the collector current of the opto-coupler output transistor increases, charging of C_{in1} will take somewhat longer time, but discharging will be faster. The opposite results if the collector current is decreased instead. Furthermore, the output transistor of the opto-coupler is equipped with a electrical control input (common transistor base, intended for biasing). The switch-transistor drain current is measured, filtered and then fed to this input of the opto-coupler (more correct: the voltage across a resistor, in series with the switch-transistor, is measured). The average MOSFET drain current is limited this way.

Following the oscillator, another inverter is placed just to invert the oscillator output signal. Then the MOSFET drive circuit follows. To be able to deliver a sufficiently high gate current at turn-on, three inverters connected in parallel are used. At turn-on, the gate current flows through the diode 183. At turn-off, the gate current is drawn through the transistor 131. The reason for using a transistor to support turn-off, is that it is harder for integrated logic circuits to sink current compared to deliver current. The problem arising if a too high current is sunk is that the output voltage of the inverter increases. The turn-on gate current can be adjusted by tuning the potentiometer 171, denoted “strömbegr”, which means current limitation. Note that it is not the MOSFET drain current which is limited, but the gate current. A limitation of the gate current corresponds to a limitation of the drain current time derivative, i.e. the drain current rise time is controlled by the potentiometer 171.

Preparations and laboratory exercises

Prepare by the laboratory work by doing exercise 1 below. Also derive the sets of expressions for exercises 3, 4 and 5 below so that you establish a work flow in such a way that you just have to insert the actual levels of the measured quantities that you obtain at the laboratory session.

1. Analyse the circuit together with your laboratory colleague. Do this well before the first laboratory session so you can ask adequate questions. Focus especially on the main circuit including input filters voltage doubling rectifier and snubber circuits.

2. The switch mode power supply is equipped with test points. Verify the operation by studying the waveforms.

   Investigate the following:

   - AC current waveforms before and after the first differential-mode (DM) RC filter, (test points 1&2 and 2&3).
   - The polarity and magnitude of MOSFET drain-source voltage waveform (test points 5&7) and how that relates to MOSFET on-state and off-state.
   - The polarity and magnitude of primary winding voltage waveform (test points 4&5), and how that relates to MOSFET on-state and off-state.
   - The polarity and magnitude of secondary winding voltage waveform (test points 23&25 and 21&23) and how that relates to Flyback diodes on-state and off-state.
   - Flyback diodes currents waveforms (test points 25&26 and 22&21) and how that relates to MOSFET the diodes on-state and off-state.

3. Estimate the losses of the input rectifier of the power supply.

   Assume that the forward voltage drop for one of the rectifier diodes is written:

$$v_D(t)=V_{D0}+R_D\cdot i_D(t)$$

   Where V_{D0}=0.7 V and R_D=50 mΩ.

   The instantaneous power corresponding to the losses of a single diode is written:

$$p_D(t)=v_D(t)\cdot i_D(t)=V_{D0}\cdot i_D(t)+R_D\cdot i_D^2(t)$$

   The diode current consists of pulses. Assume that one such pulse is sinusoidal. Measure the time duration, t_p, and its amplitude, $\hat{i}_D$. The diode current is thus written:

$$i_D(t)=\begin{cases}\hat{i}_D\cdot\sin(\omega_p\cdot t) & 0\le t<t_p\\ 0 & t_p\le t<T_n\end{cases}$$

   A sinus wave can represent each pulse for the duration from 0 to π

$$\omega_p\cdot t_p=\pi$$

   The average losses for one rectifier diode are calculated according to:

$$P_D=\frac{1}{T_n}\cdot\int_0^{T_n}p(t)\cdot dt=\frac{1}{T_n}\cdot\int_0^{t_p}p(t)\cdot dt$$

   Derive an expression for and calculate the losses for the entire rectifier bridge.

4. Calculate the losses of the Flyback-diodes. These are of type Philips BYW 29. The parameters V_{D0} and R_D are obtained from Fig. 9 (150 °C) of the datasheet. Note that the diode currents are described by

$$i_D(t)=k\cdot t+m$$

Where *k* is negative and *m* is positive. The average current cannot be used for this calculation.

5. Calculate the number of winding turns of the switch transformer. Measure the voltage and the current time derivative on the secondary side of the transformer. Out of these measurements, the magnetising inductance of the secondary is calculated. Assume that the leakage inductance is low, which means that the magnetising inductance is equal to the self-inductance. From the data sheet "Philips components / ETD cores and accessories" attached, you can find the core used (ETD44-grade 3C80-airgap of 500μm), and its A_L-value and effective cross sectional area (A_e). This directly gives the number of secondary winding turns (equation (5.77)). From the data given, the peak magnetic flux density is calculated according to equation (5.46). Compare to flux density limits specified by the manufacturer. The number of winding turns for the primary is calculated from the voltage ratio between the primary and secondary.

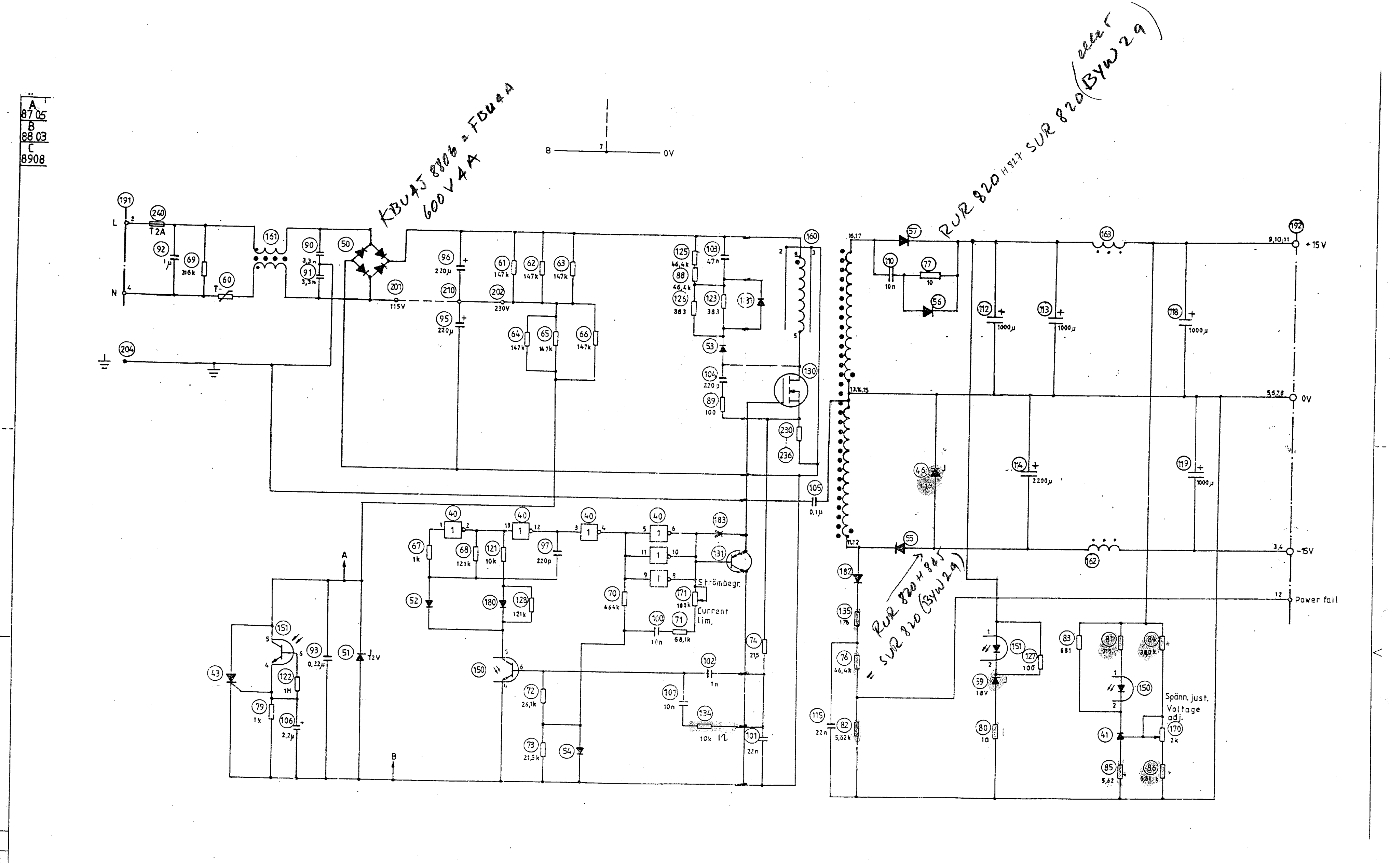
The report should contain

- A detailed description of the switch mode power supply (SMPS), especially the main circuit. The following items must be thoroughly explained:

  1. Explain the operation of the common mode filter at the SMPS input.
  2. Explain how the voltage doubling circuit at the input rectifier works.
  3. What is the main reason for using MOSFET-technology for SMPS?
  4. How high is the transformer primary voltage when the switch-transistor is conducting and blocking, respectively? How is the switch-transistor selection affected?
  5. How high is the transformer secondary voltage when the switch-transistor is conducting and blocking, respectively? How is the Flyback-diode selection affected?
  6. Explain the operation of the snubbers.

- Presentation and discussion of the calculations made above.

Schematics and datasheets for the laboratory exercise


A 8705
B 8803
C 8908
KBU4J 8806 = FBU4A
600V 4A
RUR 820 H827 SUR 820 (BYW29
eller
RUR 820 H825
= SUR 820 (BYW29)
B
0V
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N
T2A
1µ
316k
3,3n
115V
230V
220µ
147k
46,4k
383
38,3
47n
220p
100
0,1µ
1000µ
2200µ
+15V
0V
-15V
Power fail
10n
10
1k
121k
10k
220p
464k
100k
Strömbegr.
Current lim.
68,1k
1n
215
22n
0,22µ
12V
1M
2,2µ
26,1k
21,5k
176
5,62k
18V
681
383k
Spänn. just.
Voltage adj.
2k
5,62
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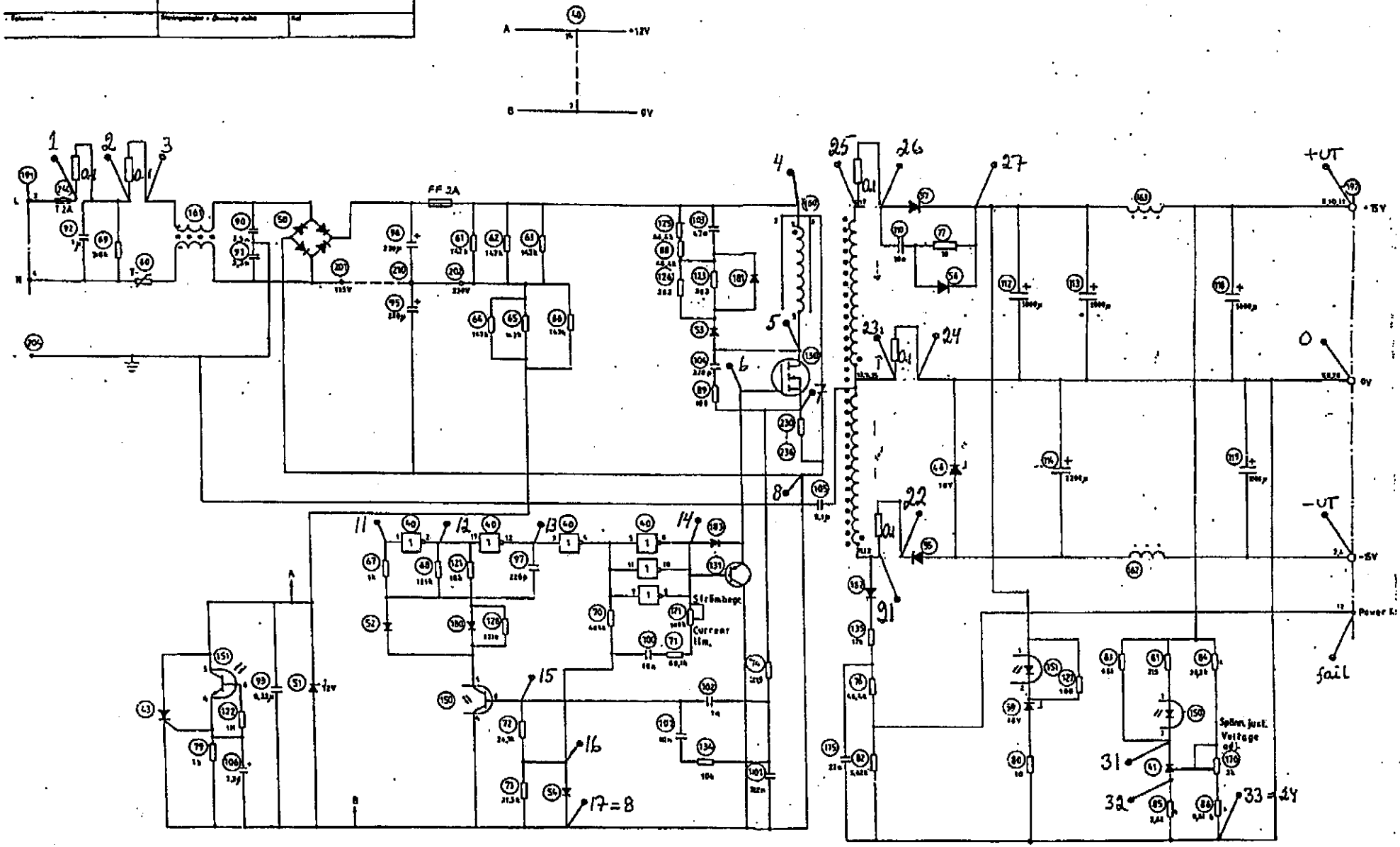
MEP EKA/KCYKR	1911-BMJ 171 009 Ux
K. 8705 L. Fengaer	See below
	PRINTED BOARD ASSEMBLY



Rectifier diodes ultrafast — BYW29 series

GENERAL DESCRIPTION

Glass passivated high efficiency rectifier diodes in a plastic envelope, featuring low forward voltage drop, ultra-fast recovery times and soft recovery characteristic. They are intended for use in switched mode power supplies and high frequency circuits in general where low conduction and switching losses are essential.

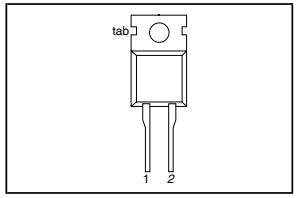
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	MAX.	MAX.	UNIT
	BYW29-	100	150	200	
V_{RRM}	Repetitive peak reverse voltage	100	150	200	V
V_F	Forward voltage	0.895	0.895	0.895	V
$I_{F(AV)}$	Forward current	8	8	8	A
t_{rr}	Reverse recovery time	25	25	25	ns

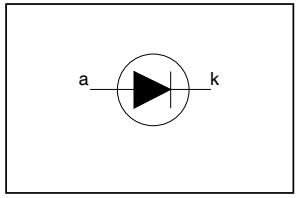
PINNING - TO220AC

PIN	DESCRIPTION
1	cathode (k)
2	anode (a)
tab	cathode (k)

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.			UNIT
				-100	-150	-200	
V_{RRM}	Repetitive peak reverse voltage		-	100	150	200	V
V_{RWM}	Crest working reverse voltage		-	100	150	200	V
V_R	Continuous reverse voltage		-	100	150	200	V
$I_{F(AV)}$	Average forward current[1]	square wave; $\delta = 0.5$; $T_{mb} \leq 128$ ˚C	-	8			A
		sinusoidal; a = 1.57; $T_{mb} \leq 130$ ˚C	-	7.3			A
$I_{F(RMS)}$	RMS forward current		-	11.3			A
I_{FRM}	Repetitive peak forward current	t = 25 µs; $\delta = 0.5$; $T_{mb} \leq 128$ ˚C	-	16			A
I_{FSM}	Non-repetitive peak forward current	t = 10 ms	-	80			A
		t = 8.3 ms sinusoidal; with reapplied $V_{RWM(max)}$	-	88			A
I^2t	I^2t for fusing	t = 10 ms	-	32			A^2s
T_{stg}	Storage temperature		-40	150			˚C
T_j	Operating junction temperature		-	150			˚C

1 Neglecting switching and reverse current losses

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base		-	-	2.7	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	in free air	-	60	-	K/W

STATIC CHARACTERISTICS

$T_j = 25$ ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_F	Forward voltage	$I_F = 8$ A; $T_j = 150$˚C	-	0.80	0.895	V
		$I_F = 8$ A	-	0.92	1.05	V
		$I_F = 20$ A	-	1.1	1.3	V
I_R	Reverse current	$V_R = V_{RWM}$; $T_j = 100$ ˚C	-	0.3	0.6	mA
		$V_R = V_{RWM}$	-	2	10	µA

DYNAMIC CHARACTERISTICS

$T_j = 25$ ˚C unless otherwise stated

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Q_s	Reverse recovery charge	$I_F = 2$ A; $V_R \geq 30$ V; $-dI_F/dt = 20$ A/µs	-	4	11	nC
t_{rr}	Reverse recovery time	$I_F = 1$ A; $V_R \geq 30$ V; $-dI_F/dt = 100$ A/µs	-	20	25	ns
I_{rrm}	Peak reverse recovery current	$I_F = 10$ A; $V_R \geq 30$ V; $T_j = 100$ ˚C; $-dI_F/dt = 50$ A/µs	-	1	2	A
V_{fr}	Forward recovery voltage	$I_F = 1$ A; $dI_F/dt = 10$ A/µs	-	1	-	V

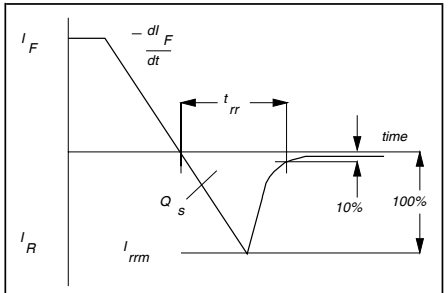


Fig.1. Definition of t_{rr}, Q_s and I_{rrm}

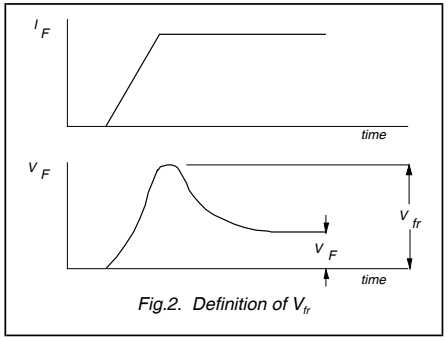


Fig.2. Definition of V_{fr}

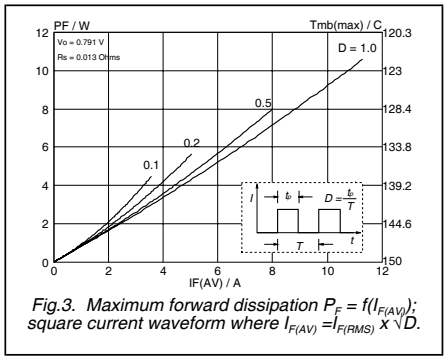


Fig.3. Maximum forward dissipation $P_F = f(I_{F(AV)})$; square current waveform where $I_{F(AV)} = I_{F(RMS)} \times \sqrt{D}$.

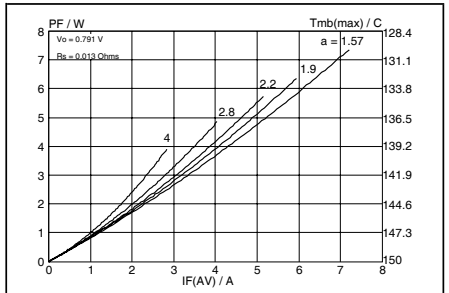


Fig.4. Maximum forward dissipation $P_F = f(I_{F(AV)})$; sinusoidal current waveform where a = form factor = $I_{F(RMS)} / I_{F(AV)}$.

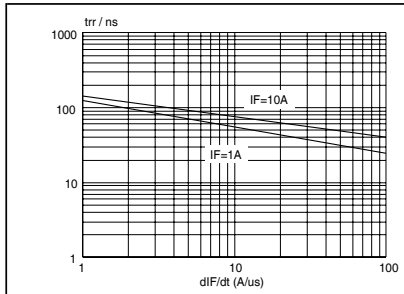


Fig.5. Maximum t_{rr} at T_j = 25 ˚C.

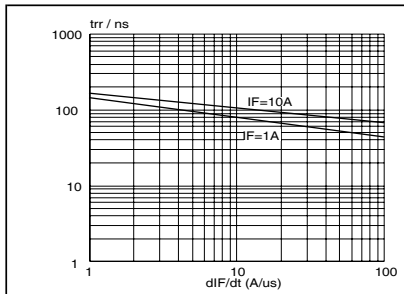


Fig.6. Maximum t_{rr} at T_j = 100 ˚C.

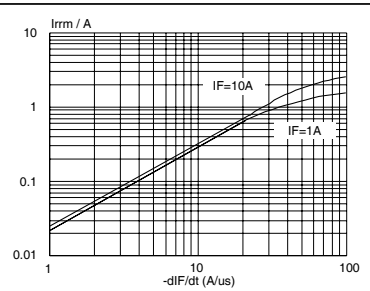


Fig.7. Maximum I_{rrm} at T_j = 25 ˚C.

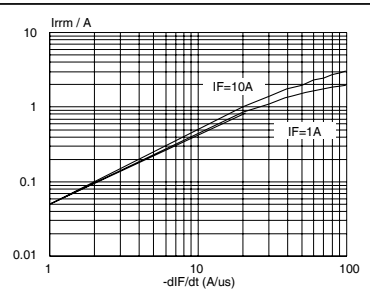


Fig.8. Maximum I_{rrm} at T_j = 100 ˚C.

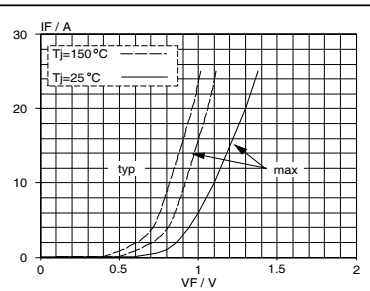


Fig.9. Typical and maximum forward characteristic $I_F = f(V_F)$; parameter T_j

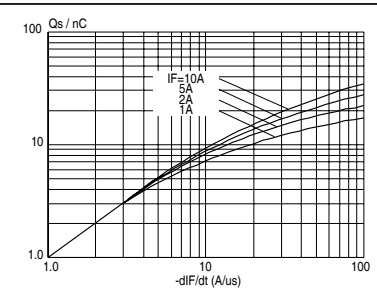


Fig.10. Maximum Q_s at T_j = 25 ˚C.

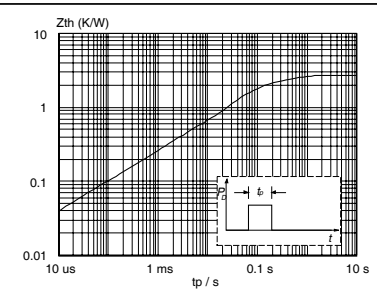


Fig.11. Transient thermal impedance; $Z_{th\ j\text{-}mb} = f(t_p)$.

ETD cores and accessories ETD44

Dimensions in mm

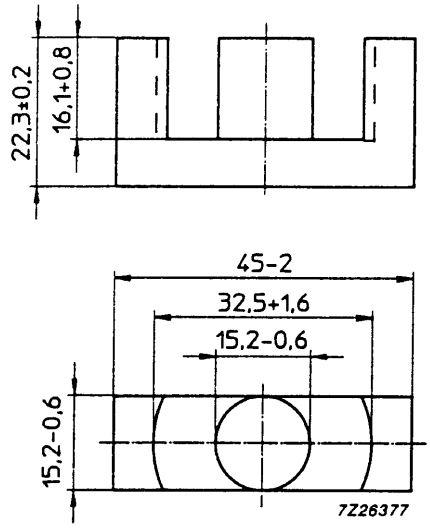


Fig.1 ETD44 core half.

EFFECTIVE CORE PARAMETERS

SYMBOL	PARAMETER	VALUE	UNIT
$\Sigma(l/A)$	core factor (C1)	0.589	mm^{-1}
V_e	effective volume	17800	mm^3
l_e	effective length	103	mm
A_e	effective area	173	mm^2
A_{min}	minimum area	172	mm^2
	mass of core half	≈ 47	g

CORE HALVES

GRADE	AIRGAP (μm)	A_L* (nH)	μ_e	ORDERING CODE
3C80	≈ 0	3500 ± 25%	≈ 1650	4312 020 3710
	100	≈ 1400	≈ 660	4312 020 3759
	200	≈ 900	≈ 425	4312 020 3711
	500	≈ 460	≈ 220	4312 020 3712
	800	≈ 320	≈ 150	4312 020 3760
3C85	≈ 0	3500 ± 25%	≈ 1650	4312 020 3730
	100	≈ 1400	≈ 660	4312 020 3731
	200	≈ 900	≈ 425	4312 020 3732
	500	≈ 460	≈ 220	4312 020 3733
	800	≈ 320	≈ 150	4312 020 3734
3F3	≈ 0	3200 ± 25%	≈ 1500	4312 020 3803
	100	≈ 1350	≈ 640	4312 020 3817
	200	≈ 900	≈ 425	4312 020 3818
	500	≈ 460	≈ 220	4312 020 3819
	800	≈ 320	≈ 150	4312 020 3820

* measured in combination with an ungapped core half, clamping force 50 ± 20 N

ETD cores and accessories

ETD44

PROPERTIES OF CORE SETS UNDER POWER CONDITIONS

GRADE	B (mT) at H = 250 A/m; f = 25 kHz; T = 100 °C	P_V (W) at f = 25 kHz; $\hat{B}$ = 200 mT; T = 100 °C	P_V (W) at f = 100 kHz; $\hat{B}$ = 100 mT; T = 100 °C	P_V (W) at f = 400 kHz; $\hat{B}$ = 50 mT; T = 100 °C
3C80	≥ 320	≤ 3.6	–	–
3C85	≥ 320	≤ 2.5	≤ 3.0	–
3F3	≥ 320	–	≤ 2.0	≤ 3.7

ETD cores and accessories

ETD44

COIL FORMER DATA

Coil former material:	polybuteleneterephtalate (PBT), glass reinforced, flame retardent in accordance with UL94V-0
Pin material:	CuSn, SnPb plated
Maximum operating temperature:	130 °C
Resistance to soldering heat:	400 °C, 2 s
Solderability:	IEC 68-2-20, Part 2, Test TA, method 1

Dimensions in mm

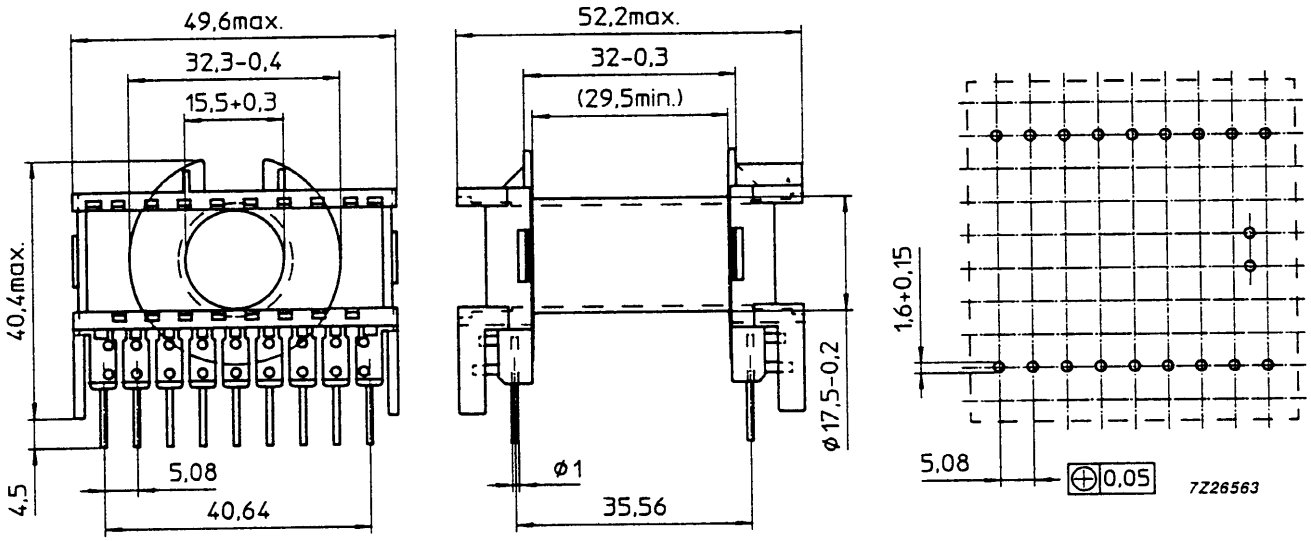


Fig.2 ETD44 coil former.

WINDING DATA

NUMBER OF SECTIONS	NUMBER OF PINS	WINDING AREA (mm^2)	WINDING WIDTH (mm)	WINDING LENGTH (mm)	ORDERING CODE
1	18	214	29.5	77	4322 021 3387

ETD cores and accessories

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MOUNTING PARTS

ITEM	FIG. NO.	ORDERING CODE	REMARKS
mounting clip	3	4322 021 3391	stainless steel
earthing clip	4	4322 021 3396	CuNiZn alloy, dip soldered

Dimensions in mm

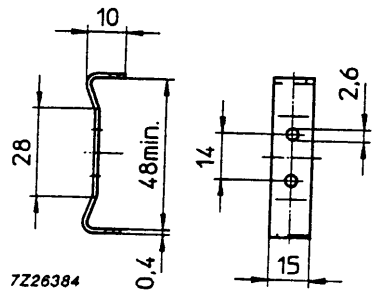

Fig.3 Mounting clip.

Dimensions in mm

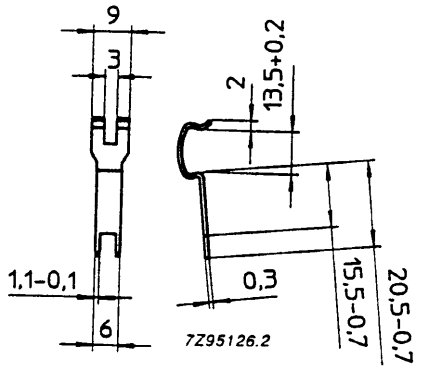

Fig.4 Earthing clip.